

CLAIMS

What is claimed is:

1. A method of forming a ferroelectric memory device, comprising:
forming a transistor on a semiconductor substrate, the transistor comprising a source
5 region, a drain region, and a gate electrode;
forming a first interlayer insulating layer over the transistor and the substrate;
forming first contact holes in the first interlayer insulating layer to expose the source
and drain regions;
forming a conductive layer on the first interlayer insulating layer and within the first
10 contact holes;
patterning the conductive layer to form a buried contact structure and a bit line,
wherein the buried contact structure is electrically connected to the source or drain region
through one of the first contact holes, and wherein the bit line is electrically connected to the
other source or drain region through one of the first contact holes;
15 forming a blocking layer on the buried contact structure, the bit line, and the first
interlayer insulating layer to prevent oxygen diffusion;
forming a second interlayer insulating layer on the blocking layer;
form a second contact hole extending through the second interlayer insulating layer
and the blocking layer to expose a top surface of the buried contact structure; and
20 forming a ferroelectric capacitor on the second interlayer insulating layer, wherein the
ferroelectric capacitor is electrically connected to the buried contact structure through the
second contact hole.
2. The method according to claim 1, wherein the conductive layer is formed by
25 stacking a tungsten (W) layer on an adhesive layer/barrier layer of titanium/titanium nitride
(Ti/TiN).
3. The method according to claim 1, wherein a diameter of the second contact
hole is larger than a diameter of the first contact hole.
- 30 4. The method according to claim 1, wherein the blocking layer is made of
silicon oxynitride (SiON), silicon nitride (SiN), or aluminum oxide.
5. The method according to claim 1, wherein forming the ferroelectric capacitor
comprises:

forming a lower capacitor electrode in the second contact hole and on the second interlayer insulating layer;

forming a ferroelectric layer on the lower capacitor electrode;

forming an upper capacitor electrode on the ferroelectric layer; and

5 patterning the upper capacitor electrode, the ferroelectric layer, and the lower capacitor electrode.

6. The method according to claim 1, further comprising:

10 forming a reaction barrier layer on the ferroelectric capacitor and the second interlayer insulating layer;

forming a third interlayer insulating layer on the reaction barrier layer;

forming a first interconnection line on the third interlayer insulating layer;

forming an inter-level dielectric film on the first interconnection line; and

15 forming a second interconnection line on the inter-level dielectric film, the second interconnection line being electrically connected to the upper capacitor electrode.

7. The method according to claim 6, wherein the reaction barrier layer is made of aluminum oxide or titanium dioxide.

20 8. A method of forming a ferroelectric memory device, comprising:

forming a transistor on a semiconductor substrate;

forming an interlayer insulating layer over the transistor and the substrate;

25 forming a buried contact structure and a bit line on the first interlayer insulating layer; the buried contact structure and the bit line electrically connected to source and drain regions of the transistor, respectively;

forming a blocking layer over the first interlayer insulating layer, the buried contact structure, and the bit line to prevent oxygen diffusion;

forming a second interlayer insulating layer on the blocking layer; and

30 forming a ferroelectric capacitor in electrical communication with the buried contact structure.

9. The method according to claim 8, wherein forming the buried contact structure and the bit line comprises:

patterning the first interlayer insulating layer to form first contact holes that expose

the source and drain regions;

forming a conductive material in the first contact holes and on the first interlayer insulating layer; and

5 patterning the conductive material such that a portion thereof remains in the contact holes and on a region of the insulating layer around the contact holes.

10. The method according to claim 8, wherein forming the ferroelectric capacitor comprises:

10 patterning the second interlayer insulating layer to form a second contact hole that exposes the buried contact structure;

forming a lower capacitor electrode in the second contact hole and on the second interlayer insulating layer;

forming a dielectric film on the lower capacitor electrode;

forming an upper capacitor electrode on the dielectric film; and

15 patterning the upper capacitor electrode, the dielectric film, and the lower capacitor electrode.

11. The method according to claim 10, wherein a diameter of the second contact hole is larger than a diameter of the first contact hole.

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12. The method according to claim 10, further comprising:

forming a reaction barrier layer on the ferroelectric capacitor and the second interlayer insulating layer;

forming a third interlayer insulating layer on the reaction barrier layer;

25 forming a first interconnection line on the third interlayer insulating layer;

forming an inter-level dielectric film on the first interconnection line; and

forming a second interconnection line on the inter-level insulating layer, the second interconnection line being electrically connected to the upper electrode.

30 13. The method according to claim 9, wherein the conductive material is formed by sequentially stacking a titanium/titanium nitride (Ti/TiN) adhesive layer/barrier layer and a tungsten (W) layer.

14. The method according to claim 8, wherein the blocking layer is made of

silicon oxynitride (SiON), silicon nitride (SiN), or aluminum oxide.

15. The method according to claim 12, wherein the reaction barrier layer is made of aluminum oxide or titanium oxide.

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16. A method of forming a ferroelectric memory device, comprising:
forming a first interlayer insulating layer on a semiconductor substrate;
forming a buried contact structure on the first interlayer insulating layer, the buried
contact structure being electrically connected to the substrate via a first contact hole
10 penetrating through a predetermined area of the first interlayer insulating layer;
forming a blocking layer on the buried contact structure and the first interlayer
insulating layer to prevent oxygen diffusion of the buried contact structure;
forming a second interlayer insulating layer on the blocking layer; and
forming a ferroelectric capacitor on the second interlayer insulating layer, the
15 ferroelectric capacitor being electrically connected to the buried contact structure through a
second contact hole penetrating through a predetermined area of each of the second interlayer
insulating layer and the blocking layer.

17. The method according to claim 16, wherein the blocking layer is made of
20 silicon oxynitride (SiON), silicon nitride (SiN), or aluminum oxide.

18. The method according to claim 16, wherein a diameter of the second contact
hole is larger than a diameter of the first contact hole.

19. The method according to claim 19, wherein the buried contact structure is
25 made of tungsten (W).

20. The method according to claim 16, wherein the bit line and buried contact
structure are formed concurrently using a conductive material.

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